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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BAHTA, KIDEST	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,721	ZHANG ET AL.	
	Examiner	Art Unit	
	Kidest Bahta	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Diard (US 7,075,541).

Regarding claim 1, Diard discloses a plurality of Island Processing Engines, wherein each IPE receives an island data set and further comprises a plurality of parallel execution units (abstract, column 1, lines 24-34, column 1, line 46 to column 2 Figs, 8 and 9); wherein each one of the pluralities of execution units resolves a data portion derived from the island data set (abstract, column 1, lines 24-34, column 1, line 46 to column 2 Figs, 8 and 9).

Regarding claims 3-5, Diard discloses,

3. The LCP solver of claim 1 wherein each IPE further comprises: an IPE memory storing the island data set (abstract, column 1, lines 24-34, column 1, line 46 to column 2 Figs, 8 and 9); an Island Control Unit (ICU) logically controlling the transfer of data from the IPE memory to the plurality of execution units (abstract, column 1, lines 24-34, column 1, line 46 to column 2 Figs, 8 and 9).

4. The LCP solver of claim 3 wherein each execution unit further comprises: an associated memory storing a respective data portion (Fig. 1, element 123a).

5. The LCP solver of claim 3 wherein each IPE further comprises: a Content Addressable Memory (CAM) operatively connected to the ICU, such that by inter-operation of the ICU and CAM each respective data portion is derived from the island data set (abstract, column 1, lines 24-34, column 1, line 46 to column 2 Figs, 8 and 9).

3. Claims 6-7 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith (US 2003/0179205).

Regarding claim 6, Smith discloses a Central Processing Unit (CPU), a main memory, and one or more peripherals including a display (Abstract); wherein the main memory stores an initial data set related to a physics-based problem arising from execution of the main application (Fig. 2, Fig. 7); the system further comprising a Linear Complementarity Problem (LCP) solver executing a projected iterative descent method adapted to resolve LCPs derived from the initial data set using a plurality of execution units arranged in parallel (page 3, Par. 32 and 42)

Regarding claim 22, Smith discloses a memory storing a data set related to a physics-based problem, the data set comprising an LCP that defines a whole gradient vector (page 1, par. 13-18, page 2, par. 29 and 32); and a plurality of execution units arranged in parallel and each receiving one of a plurality of subspaces, each subspace corresponding to a portion of the whole gradient vector (page 1, Par. 60-61).

Regarding claim 7, Smith discloses,

7. The system of claim 6, wherein each one of the plurality of execution units comprises a circuit executing floating point operations (column 2, lines 38-46).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 8-21 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 2003/0179205) in view of Diard (US 7,075, 541).

Regarding claims 12 and 23, Smith discloses a Central Processing Unit (CPU) (page 3, lines 60-66, Fig. 2), a main memory associated with the CPU, and one or more peripherals including a display (Fig. 2); wherein the main memory stores an initial data set related to a physics-based problem arising from execution of the main application; the system further comprising a Physics Processing Unit (PPU) (Page 44,, page 1, lines Par. 13-16), the PPU comprising: a PPU memory receiving and storing at least a portion of the initial data set, including a plurality of island data sets, each island data set corresponding to a rigid body island defined in the initial data set (Page 1, Pars. 13-16, Page 3, Pars. 61-66, Abstract); and, a Linear Complementarity Problem (LCP) solver executing a computational method adapted to resolve a plurality of LCPs, each LCP

being derived from a corresponding island data set (Page 2, Pars. 29-31, Page 3, Pars. 61-66, Fig. 2);

Smith fails to discloses that wherein the LCP solver comprises a plurality of execution units resolving the plurality of LCPs in parallel.

Diard discloses that wherein the LCP solver comprises a plurality of execution units resolving the plurality of LCPs in parallel (Abstract, column 1, lines 1-6, 24-34, 46)

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to modify the teachings of Smith by incorporating using a plurality of execution units arranged in parallel as taught by Diard for the purpose of increasing the number of operations that can be carried out by the system per second, thus incrementing the processing capabilities of the system.

Regarding claims 14,16, 20, 21 and 23, Smith discloses

14. The system of claim 13, wherein at least one of the plurality of execution units comprises a vector processor (Page 1, Par. 13-18).

16. The system of claim 15 wherein each execution unit further comprises an associated memory storing a respective data portion (Fig. 2).

20. The system of claim 12, wherein the PPU is implemented as a physically separate co-processor operating in conjunction with the CPU, and the LCP solver further comprises: a plurality of Vector Processing Units (VPUs) connected in parallel

and adapted to perform multiple floating point operations to simultaneously resolve the plurality of LCPs (Page 1, pars.13-18, Page 2, pars. 29-42, Appendix 4).

21. The system of claim 20, wherein the PPU is implemented on a PCI expansion board and connected within the system via a PCI expansion slot (Page 2, par. 28 and 32).

24. The LCP solver of claim 23, wherein the logic circuit comprises a Content Addressable Memory (CAM) (Fig. 2).

Regarding claims 13, 15, 17-19, Diard discloses

13. The system of claim 12, wherein the LCP solver further comprises:

a plurality of Island Processing Engines (IPEs), each IPE receiving an island data set and further comprises a plurality of parallel execution units; wherein each one of the plurality of execution units resolves a data portion derived from the island data set (column 1, lines 24-55, column 5, lines 22-column 6, lines 40).

15. The system of claim 13 wherein each IPE further comprises:

an IPE memory storing the island data set; an Island Control Unit (ICU) logically controlling the transfer of data from the IPE memory to the plurality of execution units (column 1, lines 24-55, column 5, lines 22-column 6, lines 40, Figs. 8-9).

17. The system of claim 16 wherein each IPE further comprises:

a Content Addressable Memory (CAM) operatively connected to the ICU, such that by inter-operation of the ICU and CAM each respective data portion is

derived from the island data set (column 1, lines 24-55, column 5, lines 22-column 6, lines 40).

18. The system of claim 15 wherein the PPU further comprises:

a PPU Control Engine (PCE) controlling overall operation of the PPU; and a Data Movement Engine (DME) controlling the transfer of data between the main memory and the PPU memory and the transfer of data between the PPU memory and respective IPE memories associated with the plurality of IPEs (Abstract; column 1, line 56 – column2, line 4) .

19. The system of claim 18 wherein the PPU communicates data with at least one of the CPU and main memory via at least one protocol selected from a group of protocols defined by USB, USB2, Firewire, PCI, PCI-X, PCI-Express, and Ethernet (column 9, lines 5-36).

Regarding claim 2, Diard discloses the limitation of claim 1 but fails to disclose the limitations of claim 2. However, Smith discloses the limitation of claim 2, at least one of the plurality of execution units comprises a vector processor (column 1, lines 13-18).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to modify the teachings of Simth with the teaching of Diard for the purpose of increasing the number of operations that can be carried out by the system per second, thus incrementing the processing capabilities of the system.

Regarding claims 8-11, Smith discloses the limitation of claims 6-7 but fails to disclose the limitations of claim 8-11. However, Diard discloses the limitation of claim 8-11 as follow,

8. The system of claim 7, wherein the initial data set is divided into a plurality of island data sets; and wherein the LCP solver further comprises: a plurality of Island Processing Engines (IPEs), wherein each IPE comprises a plurality of parallel execution units and an IPE memory storing one of the plurality of island data sets (column 1, lines 24-55, column 5, lines 22-column 6, lines 40)..

9. The system of claim 8, wherein each IPE further comprises an Island Control Unit (ICU) controlling the transfer of data from the IPE memory to the plurality of execution units (column 1, lines 24-55, column 5, lines 22-column 6, lines 40).

10. The system of claim 9, wherein each one of the plurality of execution units comprises a Vector Processing Unit (VPU) having an associated VPU memory (Fig. 1).

11. The system of claim 10, wherein each IPE further comprises: a Content Addressable Memory (CAM) operatively connected to the ICU, such that by interoperation of the ICU and CAM respective data portions are derived from the island data set and transferred to a corresponding VPU for resolution ((column 1, lines 24-55, column 5, lines 22-column 6, lines 40, Figs. 1, 8 and 9).

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 2003/0179205) in view of Diard (US 7,075, 541) as applied to claims 22-23 above, and further in view of Yen (US 2004/0062443).

Regarding claim 25, Smith and Dirad discloses the limitations of claims 22 and 23 but fails to disclose the limitation of claim 25. However, Yen discloses the projected iterative descent method comprises one selected from a group consisting of a Gauss-Seidel method and a steepest descent method (page 5, Par. 52; page 6, claim 9).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to modify the teaching of Smith and Dirad with the teachings of Yen in order to determine the search direction to follow when searching the subspaces to obtain a solution.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed Kidest Bahta whose telephone number is 571-272-3737. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval IPAIRI system. Status information for published applications may be obtained from either Private PMR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-fee).

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